REMARKS

1. Request for Continued Examination

Applicants respectfully request continued examination of the above-indicated application as per 37 CFR 1.114.

2. Amendments to the Claims

Claim 13 is currently amended to limit the step of updating the linked list, i.e., step (c), to be performed before the memory is completely examined by the BIST. As described in the paragraph [0024] lines 2-7, "**Each time a defective page is found in the packet buffer 30**, the switch 10 will **pause the BIST**, **update the linked list** dynamically so as not to use the section corresponding to the defective page of the packet buffer 30, **and then continue the BIST**." It can be appreciated by those skilled in the art that the operation "**continue the BIST**" means to perform the BIST on remaining portions of the packet buffer 30. Additionally, this cited paragraph clearly points out that the **linked list updating operation** begins prior to the time at which the packet buffer 30 is completely examined by the BIST.

The limitation being added into currently amended claim 13 is substantially the same as the limitation of claim 16. Accordingly, claim 16 is canceled. In addition, claim 17 that was dependent upon claim 16 is now amended to be dependent upon the claim 13.

Claim 19 is currently amended to add the same limitation as in currently amended claim 13.

Claims 23 and 24 are newly added, which are dependent upon

previously presented independent claim 22. In particular, new claim 23 is formed according to the limitation claimed in the previously presented claim 21. New claim 24 recites that the BIST is paused when the first defective portion of the memory is identified, and this is fully supported by paragraph [24].

Claims 25 and 26 are newly entered. New claim 25 recites that the method for generating a linked list corresponding to a memory comprises steps of: **forming a linked list** for the memory, wherein the linked list comprises a plurality of entries each having a first pointer field and a second pointer field, the first pointer field for storing a pointer to a corresponding portion of the memory and the second pointer field for storing a pointer to another entry of the linked list; **performing a built-in self test (BIST) on the memory**; and each time a defective portion is found in the memory by the BIST, **pausing the BIST**, **updating the linked list** to remove an entry corresponding to the defective portion of the memory from the linked list, **and then continuing the BIST** on remaining portions of the memory. These limitations are fully supported by paragraph [0005] and paragraph [0024]. In addition, new claim 26 is formed according to the limitation claimed in previously presented claim 21.

No new matter is introduced by such amendments. Consideration of these amendments is respectfully requested.

3. Objections of drawings under 37 CFR 1.83(a):

Examiner stated that the features of the invention specified in the claims: "a portion of the memory", "updating is performed before the BIST performed", "completely through with the entirety of the memory" and "a first and a second defective portion of the memory" must be shown in the drawings.

Response:

As to the feature "a portion of the memory":

As stated in the paragraph [0004], "...A packet buffer is usually segmented into sub-blocks, where these sub-blocks are designated as "pages"...," since this is very well known in the art, the details of the packet buffer are not shown in the drawings. The paragraph [0004] further states, "... Conceptually, a linked list contains entries, wherein **each entry is associated with one page of the packet buffer**". Additionally, the paragraph [0005] states "As shown in Fig.1, the linked list with 8 entries includes a first pointer field corresponding to the pointers to the current page of an associated packet buffer (not shown), and a second pointer field corresponding to the entry associated with the next page. **Take Entry 4 as an example; it is shown in Fig.1 that the first pointer of Entry 4 corresponds to a current page (Page 4) of the packet buffer, and the second pointer of Entry 4 corresponds to the entry associated with the next page, which is Entry 5 in this case.** This same manner of association can be seen for each entry of the linked list". Accordingly, applicants assert that the feature "a portion of the memory" specified in claim 13 can be readily observed from Fig. 1 and supported by above-identified paragraphs.

As to the features "updating is performed before the BIST performed" and "completely through with the entirety of the memory":

These two features were previously specified in cancelled claim 16, **but they should be combined together as a timing feature of the linked list updating operation** rather than separated into two features. Cancelled claim 16 recited that, "the step (c) of updating is performed before the BIST performed in step (b) is completely through with the

entirety of the memory." This limitation should be interpreted as that **the step of updating the linked list is performed before the memory is completely examined by the BIST**. As described in the paragraph [0024] lines 2-7, "**Each time a defective page is found in the packet buffer 30**, the switch 10 will **pause the BIST**, **update the linked list** dynamically so as not to use the section corresponding to the defective page of the packet buffer 30, **and then continue the BIST**." Please note that, when a defective page of the packet buffer 30 is found, **the BIST is paused but this does not mean that the BIST is finished**. Accordingly, the switch 10 continues the BIST **after** the linked list is updated according to the found defective page. Namely, the linked list updating operation is performed **before** the packet buffer 30 is completely examined/checked by the BIST.

In order to avoid the feature "updating is performed before the BIST performed in step (b) is completely through with the entirety of the memory" from being misinterpreted and to overcome such objections, applicants add a timing limitation "**before the memory is completely examined by the BIST**" at the end of the step of updating the linked list, i.e., step (c), of claim 1 and cancel claim 16 since claim 16 recites an equivalent limitation. Since the limitation "before the memory is completely examined by the BIST" can be readily derived from above-identified paragraph [0024], applicants assert that this feature is not necessary to be shown in the drawings.

As to the feature "a first and a second defective portion of the memory":

As stated in paragraph [0019] lines 7-11, a reference, "a programmable BIST core for embedded DRAM" by Huang et al. concerning the details of the built-in self test (BIST), is incorporated by reference within the present application. This paragraph clearly states

that the way to detect defective portions of the memory by using BIST is very well known in the art. Furthermore, **any defective portion of the memory is just a portion of the memory**, such as a page, and it is not essential for a proper understanding of the invention. As per the descriptions "Each time a defective page is found ... and then continue the BIST" in the above-identified paragraph [0024], it can be readily appreciated that the packet buffer 30 may have two or more defective pages, and same operations (i.e., pause BIST, update linked list, and then continue BIST) are repeated at each time a defective page is found. The features "a first defective portion of the memory" and "a second defective portion of the memory" specified in the claims are intended to clearly highlight the repeated operations at each time a defective portion is identified. Therefore, applicants believe that they are not necessary to be shown in the drawings.

4. Rejections of claims under 35 U.S.C. 112:

Claims 13-18 and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing comply with the written description requirement.

Response:

Claim 13

Examiner stated that the limitations "wherein each entry of the linked list corresponds to a portion of the memory", "a portion of the memory", and "a first defective portion of the memory" in claim 13 were not described in the specification at the time the application was filed. However, applicants assert that these limitations can be readily derived from the specification at the time the application was filed. Hereinafter, further details will be explained.

The paragraph [0004] lines 4-5 state, "A packet buffer is usually

segmented into sub-blocks, where these sub-blocks are designated as "pages". The paragraph [0004] lines 9-10 state, "Conceptually, a linked list contains entries, wherein **each entry is associated with one page of the packet buffer**". Additionally, the descriptions in paragraph [0005] lines 2-12 state "As shown in Fig.1, the linked list with 8 entries includes a first pointer field corresponding to the pointers to the current page of an associated packet buffer (not shown), and a second pointer field corresponding to the entry associated with the next page. **Take Entry 4 as an example; it is shown in Fig.1 that the first pointer of Entry 4 corresponds to a current page (Page 4) of the packet buffer, and the second pointer of Entry 4 corresponds to the entry associated with the next page, which is Entry 5 in this case.** This same manner of association can be seen for each entry of the linked list". According to the above-identified paragraphs, applicants believe that the feature "wherein each entry of the linked list corresponds to a portion of the memory" and "a portion of the memory" specified in claim 13 can be readily observed from Fig. 1 and is fully supported by the specification at the time the application was filed.

In addition, the feature "a first defective portion of the memory" is clearly described in the paragraph [0024] lines 2-7. In this paragraph, "each time a defective page is found in the packet buffer 30..." means "each time **a defective page of the packet buffer 30** is found". Therefore, the feature "a first defective portion of the memory" is fully supported by the specification at the time the application was filed.

As in the foregoing explanations, it can also be readily derived from the above-identified paragraph [0024] that the linked list updating operation is performed **before** the packet buffer 30 is completely examined by the BIST. Applicants therefore assert that the limitation "before the memory is completely examined by the BIST" being added into currently amended claim 13 is also fully supported by the

above-identified paragraph [0024].

Claim 16

Claim 16 has been cancelled.

Claim 22

Examiner stated that the limitation "a first and a second defective portion of the memory" in claim 22 was not described in the specification at the time the application was filed.

Applicants assert that this limitation can be readily observed from paragraph [0024] lines 2-7. As per the descriptions "Each time a defective page is found ... and then continue the BIST" in the above-identified paragraph [0024], it can be readily appreciated that the packet buffer 30 may have two or more defective pages, and some operations (i.e., pause BIST, update linked list, and then continue BIST) are repeated at each time a defective page is found. The features "a first defective portion of the memory" and "a second defective portion of the memory" specified in claim 22 are simply intended to highlight such repeated operations when the memory has multiple defective portions. Applicants therefore assert that these limitations are fully supported by the specification at the time the application was filed.

5. Rejections of claims under 35 U.S.C. 102:

Claims 13-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (Kim) US Patent No. 6,781,898 or rejected under 35 U.S.C. 102(a) as being anticipated by Chin US Patent Pub. No. 2003/0145250.

Response:

Claims 13-15 and 17-21

As explained in both the communication, filed 06/15/2006, in response to the Office Action mailed on 03/15/2006 and the communication, filed 09/18/2006, in response to the Office Action mailed on 07/19/2006, both Kim and Chin begin to update the linked list **AFTER** the BIST is completely finished (i.e., the memory is completely examined by the BIST). Unlike Kim and Chin, the currently amended claims 13 and 19 further restrict that the step of updating the linked list begins **BEFORE** the memory is completely examined by the BIST. Accordingly, applicants assert that the currently amended claims 13 and 19 are patentably distinct from both Kim and Chin since Kim and Chin fail to teach this feature.

Claims 14, 15, 17, and 18 are dependent upon claim 13, and should be allowed if claim 13 is found allowable. Similarly, claims 20 and 21 are dependent upon claim 19, and should be allowed if claim 19 is found allowable.

Claims 22-24

Claim 22 recites that "(d) after step (c) is completed, continuing the BIST to identify a second defective portion of the memory." Please note that, "continuing the BIST" means that the BIST is **NOT** completely finished. In other words, the limitation "after step (c) is completed, continuing the BIST to identify a second defective portion of the memory" indicates that the step of updating the linked list begins **BEFORE** the memory is completely examined by the BIST. According to this significant difference, applicants assert that claim 22 is patentably distinct from both Kim and Chin since Kim and Chin update the linked list **AFTER** the BIST is completely finished.

Claims 23 and 24 are dependent upon claim 22, and should be allowed if claim 22 is found allowable.

6. Patentability of new claims 25-26

Claim 25

Claim 25 recites that "each time a defective portion is found in the memory by the BIST, **pausing** the BIST, **updating the linked list** to remove an entry corresponding to the defective portion of the memory from the linked list, **and then continuing the BIST** on remaining portions of the memory." As explained previously, it can be readily derived from the limitations specified in claim 25 that the operation of updating the linked list begins **BEFORE** the time at which the BIST is completely finished. In addition, both Kim and Chin fail to teach the features "pausing the BIST" and "continuing the BIST." According to the abovementioned arguments, applicants believe that the new claim 25 should be allowable.

Claim 26 is dependent upon claim 25, and should be allowed if claim 25 is found allowable.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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